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Improving Robustness of Dual Port SRAM by finding additional bugs in design using ESPCV flow to compare Schematics v/s Verilog on 12LP GF Technology as an example

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Abstract: Robustness in design is one of the major concerns in memory design, this will be checked with the help of various verification techniques used in the industry. Functional verification is used to check whether the design meets the specification. Evolution in verification has led to the development of formal verification tools nowadays. The symbolic simulators involve the formal verification technique along with the simulation approach. This makes debugging of circuit faults easier. ESP-CV is a symbolic simulator designed for functional verification and sequential equivalence checking of custom memory design. Symbolic simulation compares two design i.e. behavioral RTL verilog and transistor-level SPICE netlist by generating testbenches for different cycles. This article includes the basic flow of ESP-CV simulation and how this flow helps in improving robustness of SRAM design. This tool is used early in the design flow because of its ability to read RTL models and Spice netlists directly. This article also diagrams the key difficulties of memory check, and proceeds to depict how symbolic simulation and its basic advancements offer points of interest for confirming full-custom circuit design.

Index terms: RTL, IMDK, FINFET, SRAM, ESP-CV

1. INTRODUCTION:

1.1 SRAM

Static random -access memory (SRAM) is the basic building block for silicon on chip (SoC) technology because of its high speed, low power consumption and compatibility with standard technology. SRAM are used in various applications like Personal computers (PC), Mobile communications, consumer electronics etc. In any chip the memory requires greater part while the memory cell array covers most of the part in memory. The speed with which read and write operation occurs in memory cell array is increasing nowadays, so the memory unit configuration is crucial advancement in VLSI design.The single port SRAM consist of six transistors basically, it is the standard memory cell. As shown in figure, it consists of two pull up transistors that are PMOSs and two pull down transistors that are NMOSs. The single port SRAM has only one port for accessing data and address. So, either it can read or write at one time. The 8T SRAM memory cell is somewhat similar to that of single port SRAM. It consists of two ports for data access and address paths. Thus, it is known as dual port memory. In this kind of memory cell each address and data ports can read and write separately. The Read and Write operation of 8T SRA is similar to that of 6T SRAM.

1.2 SYMBOLIC SIMULATION:

There are three methods presently available for functional equivalence check to the designers, these are - conventional simulation, cone-based equivalence checking, and symbolic simulation. The initial two techniques are known by everyone while the symbolic simulation is gaining interest from couple of years and is more advanced and commercially available. Each method has its advantages and the best method depends on the application kind.

Symbolic simulation is becoming more trending for full custom memory design configuration in the course of few years. In symbolic simulation symbols like 0, 1, x and z are applied as inputs in comparison to only bits to generate RTL description and SPICE level circuit. The simulator passes these symbols from input to output. Then further the output conditions are checked for all possible combination of inputs and it is observed whether the output condition matches for both the models.

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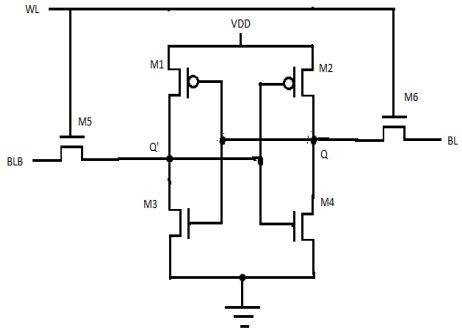

Fig. 1.: Single port SRAM

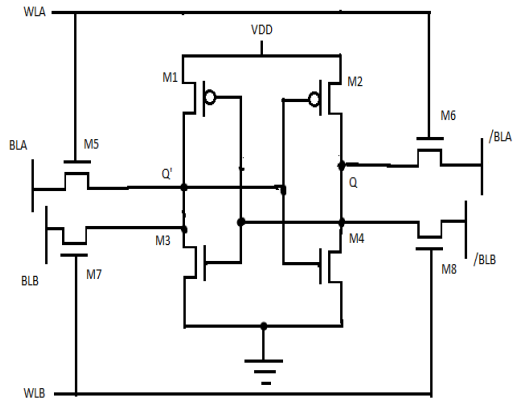

Fig. 2. Double port SRAM

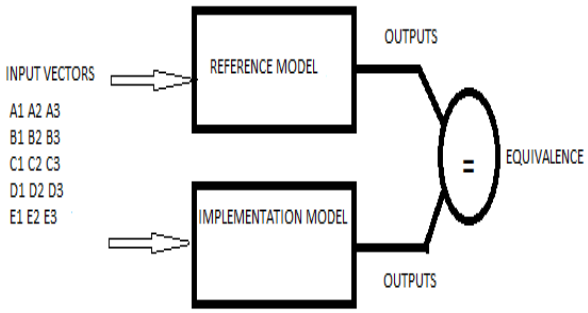

Fig. 3. Symbolic Simulation

2. ESPCV FLOW

It is very important to assert that the SRAM design is able to perform the desired functionality as per described by Verilog Reference model. In order to check for the functionality ESP simulation is being done where the transistor level Spice netlist is matched with Rtl reference verilog model. The use of Symbolic simulation for functional verification of design provides the full coverage using lesser number of symbolic cycle.It is compatible with most of the competing technologies and works absolutely fine with existing design environment.

We have been working on GF 12LP FINFET technology which provides much improvement in circuit density and performance in comparison to previous technologies. We have done ESP simulation for many instances which is Dual ported SRAM design with particular specification of wordlines, Bitlines, mux etc.

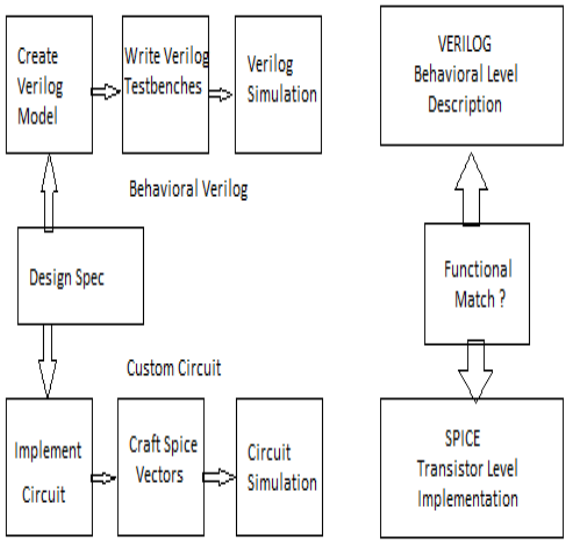

Fig. 4. Functional Equivalence Check using ESP-CV

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Here are the steps for ES-PCV simulation:

1. Setting up ESP Environment: Making directories, Loading modules and opening xterm to run the simulation. Here we have used ESP/N-2017 version of ESP-CV.

2. Generating Reference model and transistor level model: The Reference Model is the RTL reference code written in verilog. We are generating this using IMDK. The transistor level model is the SPICE netlistgenerated directly from schematic using virtuoso.

3. Generating techfile.edm and esp.tcl: The ESP-CV may not show appropriate functionality with the default models, so to get better idea we create edm file with the PDK models. All models like pfet, slvtpfet, lvtnfetetc is to be specified there. The ESP tool provides a TCL shell command line interface. Esp.tcl is a main file which is used during simulation and where netlist and verilog are being included. It also contains all other variables set for the simulation.

4. Setting up Constraints, ports and Supplies: In esp.tcl all supplies are configured including virtual nets, also it contains all ports to be matched, set variable for mentioning unmatched ports. All the testbench attributes are set with their functionality, all the constraints are set as shown in Fig. 5.

```
set_constraint POWERGATE    -set {'b 0}
set_constraint DEEPSLEEP    -set {'b 0}
set_constraint T_LOGIC      -set {'b 0}
```

Fig. 5. Setting constraints in esp.tcl

5. Start Simulation: Initially tool will read all the input files, supplies and ports will be checked. If it will have any parsing errors, log file is to be checked for unmatched ports.

6. Generating testbenches: The Testbench is generated after all ports has been matched. ESP call esptbgen to generate a testbench. The ESP tool creates testbenches with set of cycles in the order – INIT, BINCYCLE, SYMCYCLE and FLUSHCYCLE. The following testbenches are generated:
   (i) esp.tb.bin: binary testbench
   (ii) esp.tb.dit: address/data are made symbolic,
   whereas control pins are binary
   (iii) esp.tb.ptl: control pins are symbolic
   (iv) esp.tbl.2ph: checks on both phase of clock

7. Verification and Debugging: ESP-CV do the symbolic simulation which is event driven.
   ESP checks the outputs of the two models by searching the entire input vector space, if ESP finds the input vector which lead mismatch of the two models or it has searched the entire input vector space, it will stop the symbolic simulation. If the design is passed then coverage report is generated, if errors are found then debugging is done.

3. ERRORS FOUND IN DESIGN

Here, the reference instance is IN12LP_SDPB_W00064B016M04S2_HDCBTG where there are 64 words, 16 bits, mux-04 configuration with single bank having 2 subarrays.

1. Width of MCLK: As internal clock is being generated for performing different operations, the width of the clock was not appropriate for accessing farthest bank. This led to errors in the functional check.

2. Address sequence: Due to modified sequence of address in verilog there were few errors.

3. Address collission: As in Dual port we can read and write from both the ports at same time, sometimes if the address of both the ports is same then data may be lost.

4. Design issues: This is the main part which is to be focused, the schematic designed may have some manual errors. ESP-CV let you to do complete functional check and with help of waveforms we can trace the error. During the simulation we have found two errors, in different instances. The pins were swapped in the schematic due to which there was a mismatch.

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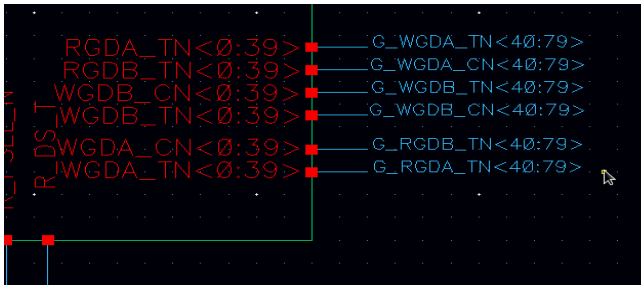

Fig. 6. Manual Errors

4. DEBBUGGING THESE ERRORS

1. The width of MCLK can be increased accordingly by providing delay to the one which generates MCLK in
timing system circuit.

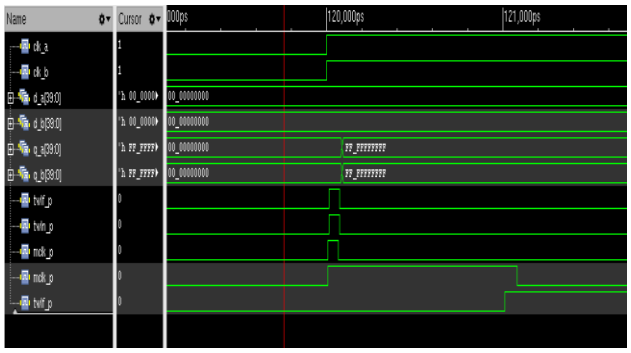

Fig. 7. Mclk width

2. The address sequence was corrected in the schematic (netlist).
3. In this case the address of one port is inverted, so that it will not access same bitcell.
4. All the design issues are corrected as per the error traced in the waveform.

5. RESULTS

The Report for the Functional mode is shown in the fig. 8. This shows that the SPICE netlist and the verilog behavioral model matches for all the testbenches. This also indicates that the design is clean. The Comparison of ESP Simulation with other Conventional techniques is also shown in the table below

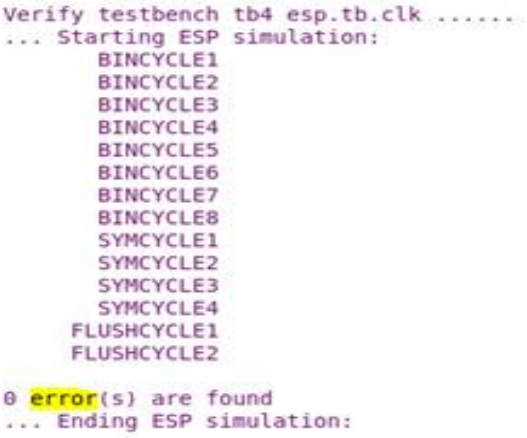

Fig. 8. Simulation Passed after Correction

Table 1. Comparison of other simulation techniques with symbolic simulation

Criteria	Other Simulation Techniques	Symbolic Simulation
Based on number of input combinations it can check.	This cannot check all the possible combination even if taken months for simulations.	It can explore all possible combinations as symbols are used to propagate through both models.
The extent to which it can find bugs.	It can miss corner case scenarios as limited test vectors are given.	As it starts early in the design, it can catch bugs almost at each corner.
Ability to observe effects of change in design	It may propagate bugs to output pins but needs to be exposed.	Automatically isolate the cause of bugs and incorrect behaviors.

6.CONCLUSION

ESP-CV gives quick and broad coverage, empowering users to quickly discover bugs and have the certainty that the Verilog reference model is practically indistinguishable to its transistor-level implementation. In practical work, we have discovered various mismatches between the circuit schematic and the RTL description, which help us a great deal to extend our understanding of the behavior description of circuit also to the circuit debug.

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