ISSN(Online) : 2456-8910
International Journal of Innovative Research in Applied Sciences and Engineering (IJIRASE)
Volume 3, Issue 1, DOI: 10.29027/IJIRASE.v3.i11.2019, 428-431 , July 2019

Optimization of Schematic Tiling Technique using Cadence SKILL Code

Kritika Sahu[1]Dr.Laxmi Kumre[2]Dr.Bhavana P. Shrivastava[3] Bidhan Kali Bhattacharyya[4]

[1]Maulana Azad National Institute of Technology, Bhopal, Madhya Pradesh
[2] Maulana Azad National Institute of Technology, Bhopal, Madhya Pradesh
[3] Maulana Azad National Institute of Technology, Bhopal, Madhya Pradesh
[4] INVECAS Technologies Pvt. Ltd., Bangalore, Karnataka

Abstract. As the world is digitizing, requisite of memory rising exponentially. The time to deliver memory is the requirement of today's world. But to design and analyze the performance of a memory is a time-consuming process. The schematic design needs to be speed up. The Tiler code is a probable solution to optimize the design process. It uses SKILL script language of Cadence Virtuoso to design symbol and schematic of a G level of a memory. It reduces tremendous amount of time and goofy errors. This paper presents the tiling technique to design memory's G level schematic and symbol.

Keywords:SRAM, DRAM, GDS, LVS, DRC, PPA, CIW

1 Introduction

Digitization is automating of manual and paper-based processes, enabled by the digitization of information. As the world is digitizing, reliance on data access has increased which led to the more requirement of memory.

The memory implies any information or data, often in binary format, that a machine or device can recall and retrieve it. A semiconductor memory is an integrated circuit designed to store digital electronic data. There are multiple memories available like SRAM, DRAM, Dual Port SRAM, Flash etc. with different technologies. The application of a memory depends on the specification of a device.

The time to deliver the product is the main concern along with the required PPA of a memory. Earlier, manual creation of a memory for few demands were feasible. But with time and demand it turn out to be tedious and time-consuming process. As manual work for such huge demand would require much labour time which leads to goofy errors and disturbance in scheduling. The trivial errors impact on LVS and DRC clean of a layout design from where the GDS is generated and forwarded to foundries for fabrication. Henceforth, a technique to customize the creation of a memory is vital.

Tiler code is a credible solution for customization of schematic generation of a memory. It is a script which can generate symbol, schematic and layout of a memory design. The script is in SKILL language which uses library of IL functions. The tool used to execute the generated .il file is Cadence Virtuoso. This optimization reduces manual effort, goofy errors and time requirement.

2 Memory Organization

As the technology scales, the PPA is main concern which leads to different memory with different architecture characteristics. The selection of memory depends on the applications and its organization depend on parameters and PPA.

If number of words increases, access time for last word also increases as RC component of wire effects. Similarly if bits increases, the capacitance load on word line gets added which also effect the performance. So its not possible to use the basic memory architecture which include wordline driver, array, control and I/O.

One of the memory architecture is Half Butterfly as shown in fig 1. As the bit requirement increases and words are manageable, half butterfly architecture would be more suitable. In these the array are divided into two sub array parts and placed on both sides of word line drivers. It reduces the load capacitance of bit lines on per word lines since it get halved. For example, if there are 20 bit lines then it would get divided into 10 bit lines on both sides of driver.

The schematic generated using Tiler code is a half butterfly with two parts: SEGIO and SEGARRAY as shown in fig 2.

The SEGIO is a functional block whose function is to generate all the desired signals like which word line should be active, among read or write operation which job need to be performed, which bank in SEGARRAY must be selected etc. by taking input from outside world like CLK, ADD, CEN, RDWEN and so on.

ISSN(Online) : 2456-8910
International Journal of Innovative Research in Applied Sciences and Engineering (IJIRASE)
Volume 3, Issue 1, DOI: 10.29027/IJIRASE.v3.i11.2019, 428-431 , July 2019

The SEGARRAY is a functional block which contain the sub array which has a bit cell where actual read and write operation occur and it is controlled by wordline driver which in turn controlled by CONTROL of SEGIO.

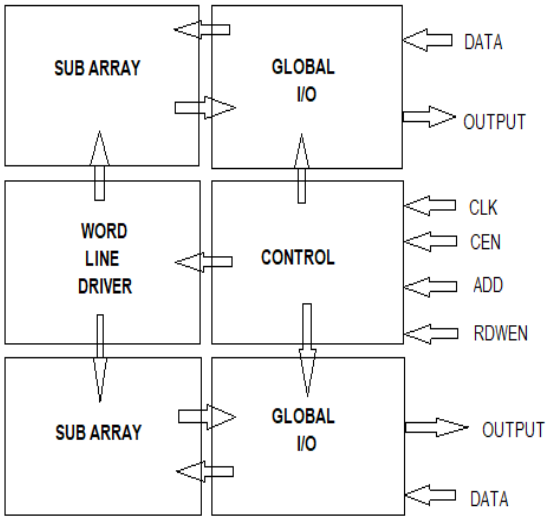

Fig1: Half butterfly

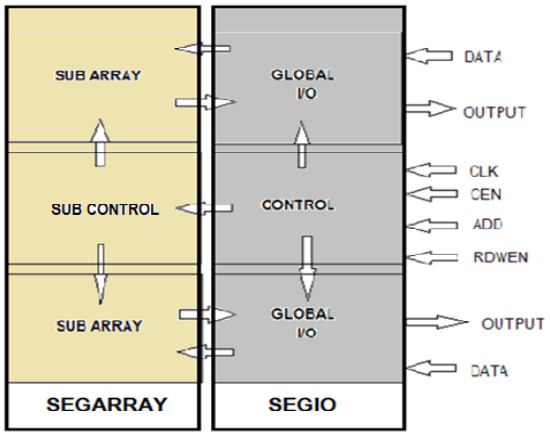

Fig2: Top level of memory generated

Since memory design is a complex in architecture, it is parted in three different level for designing which are Circuit level (C level), Placeable level (P level) and Growable level (G level).

The C level is a base of any memory design, like it includes a bit cell design. It is a level which remain same irrespective of specification of user.

The P level is a next level of C level where symbol of a particular functional block is placed to generate schematic and connection between functional block is established, as shown in fig 3. The layout is designed for this level.

The G level is upper level of P level where the symbol of P level is iterated multiple time as per the requirement to generate schematic. There can be different functional block in a schematic. It can have non-iterated schematic too like top level as shown in fig 2.

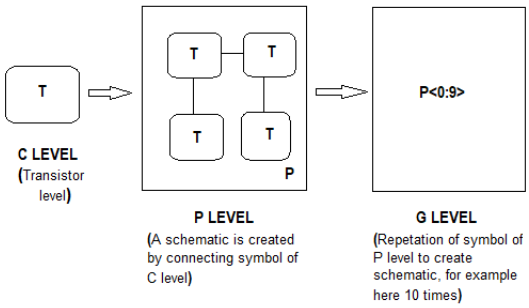

Fig3: Design level

3 Implementation

The Tiler code using SKILL, script language of Cadence, generates a schematic and symbol of a macro with utmost accuracy. It optimizes the creation of a macro with tremendous reduction in time requirement and goofy errors.

There are two ways to generate symbol and schematic:

Method 1: Generate a new symbol and schematic for a new macro

Method 2: Take already generated macro as reference for creating a new macro

The method 2 is preferred as there were already available some macros.

The following are the methodology to generate symbol and schematic of an macro:

A. The methodology to generate a symbol of each functional block of a macro:
   i. Take a reference macro of a required characteristics.

ISSN(Online) : 2456-8910
International Journal of Innovative Research in Applied Sciences and Engineering (IJIRASE)
Volume 3, Issue 1, DOI: 10.29027/IJIRASE.v3.i11.2019, 428-431 , July 2019

ii. Analyse which pins of a reference symbol depends on different parameters of a memory.
iii. Then make that pin depended on parameters.
iv. With the help of SKILL then list all the pins with its coordinates in a variable, let say X.
v. Then in that variable parse the dependent variable and do changes as per requirement. The changes will reflect in that variable, X
vi. Then create a new symbol of required parameter of same characteristics taking list of pins from modified X.
vii. Repeat all above steps for different symbol generation.
viii. Once the code is written, the .il file is loaded in CIW window.

B. The methodology to generate schematic of each functional block of a macro:
i. Open the symbol in read mode to be placed in schematic.
ii. Open the schematic to be generated in either write or append mode.
iii. Place different generated symbol at appropriate position in schematic cell view to generate desired functional block.
iv. Create wires for each symbol ports.
v. Label the wire appropriately.
vi. Create input, output or inputoutput pin for desired wire or symbol ports.
vii. Save and check the schematic generated for a particular functional block.
viii. Repeat above steps to generate schematic of different functional block.
ix. Load the .il file in CIW window.

4 Results

The Tiler code is generated including multiple files of .il format, each performing different functionality. There is one user configuration file which includes all other files. This user configuration file is loaded in CIW (Command Interpreter Window) window, as shown in fig4, of Cadence Virtuoso.

The following are some symbol and schematics of G level of half- butterfly structure of Dual Port SRAM generated using Tiler code:

Fig4: Symbol of Top-level of a macro

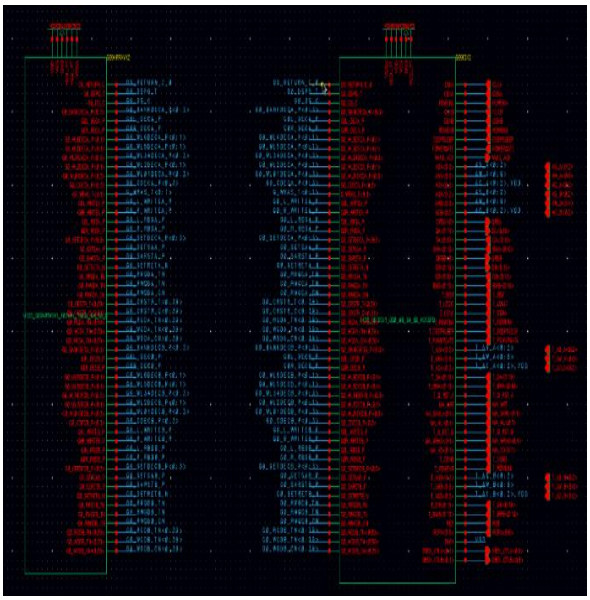

Fig5: Top-Level schematic of a macro

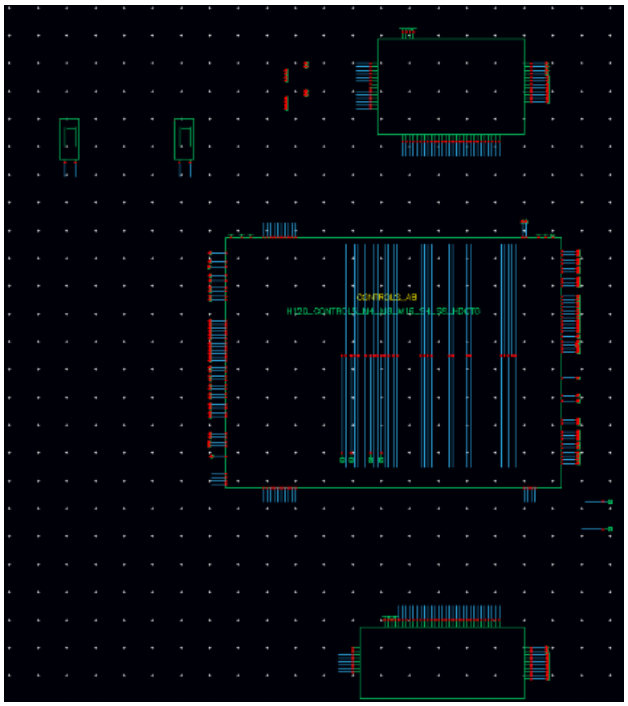

Fig6: Schematic including Control, Global I/O on either side of control

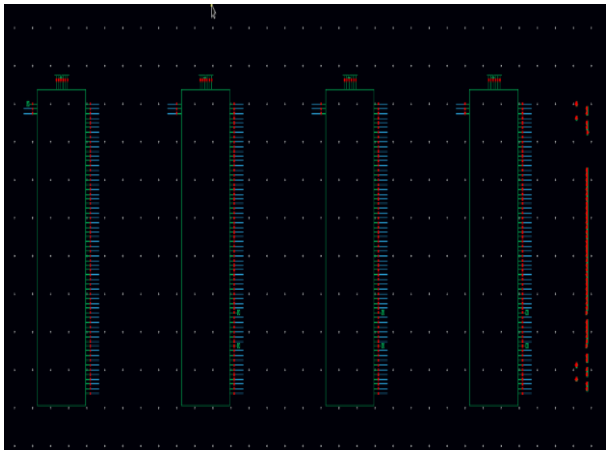

Fig7: Bank which includes local I/O and sub-control

5 Conclusion

Automating the Virtuoso Design Environment reduces dependencies on manual job. Leveraging the SKILL language in the design flow will save design team valuable time and also reduces the risk of making critical mistakes. It will improve operational efficiency and there is a great advantage in seeking increasing speed and scale.

References

1. T.J.Barnes, 1990, "SKILL:a CAD system extension language", 27th Acm/IEEE Design Automation.
2. Chandan Sharma, 2016, "An integrated tool for automation of custom IC design flow", 2016 International Conference on Computing Communication Control and automation (ICCUBEA).
3. SobhanaTayenjam, Venkata Narayana Rao Vanukuru, S.Kumaravel, 2017, "A Pcell design methodology for automatic layout generation of spiral inductor using SKILL script " , 2017 International conference on Microelectronics Devices, Circuits and Systems (ICMDCS).
4. Cadence SKILL Language User Guide, Version ICADV12.2, January 2016
5. Cadence SKILL Development Help, Version ICADV12.1, January 2013